REMARKS

Claims 1-31 and 99 are pending in the present application.

Claims 1-3, 7-16, 18-25, 29-31 and 99 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,338,996 ("Iizuka"). Applicants respectfully traverse this rejection.

Claim 1 recites a capacitor comprising, *inter alia*, "a bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," as recited in claim 1 (emphasis added). Iizuka does not disclose all the limitations of claim 1.

The Office Action erroneously relies upon the discussion of prior art in Iizuka because it is the prior art that Iizuka is *teaching away* from. The prior art discussed in Iizuka discloses "the BST thin film is crystallized with the RTA processing at 700 degrees C. in nitrogen" and that "a noble metal upper electrode using Ru or the like is formed to obtain a thin film capacitor." Col. 1, lines 30-34. In outlining the reasons for teaching away from the prior art, Iizuka discloses that "crystallization of the boundary between the lower electrode and the BST thin film is not sufficient" and that "formation of the upper electrode causes a damage to the boundary between the lower electrode and the BST thin film and crystallization of this boundary is also insufficient." Col. 1, lines 40-45.

By contrast, Iizuka discloses "a semiconductor memory device production method" to "reduce a leak current at room temperature and suppress leak current increase during an operation at a high temperature." Col. 2, lines 23-25. Specifically,

Iizuka discloses "a capacitor formed by a high dielectric insulation film and a noble metal upper electrode which are successively layered on a noble metal lower electrode, the method being characterized in that the formation of the capacitor is followed by anneal in a nitrogen atmosphere of 1 atmospheric pressure at temperature of 300 to 400 degrees." Col. 2, lines 28-34. Specifically, in the first embodiment, Iizuka teaches that "*[a]fter* forming the high dielectric thin film capacitor, [an] anneal is performed . . . in a nitrogen atmosphere." Col. 4, lines 28-31. (Emphasis added). In the second embodiment, Iizuka discloses, again, that "*[a]fter* the high dielectric thin film capacitor is formed, [an] anneal is performed in a gas mixture of oxygen (5% or below) and nitrogen." Col. 4, lines 55-59. (Emphasis added). Hence, Iizuka teaches that in the nitrogen atmosphere-containing *and* the oxygen plus nitrogen atmosphere-containing anneals, *both* anneals are conducted *after* the high dielectric thin film capacitor is formed. Iizuka does *not* disclose an *annealed* dielectric layer *and* a separately annealed top conducting layer. The final structure in Iizuka is different from the claimed invention as a result of using only a single anneal process.

Since Iizuka does not disclose all the limitations of claim 1, claim 1 and claims 2-3, 7-16, 18-25 and 29-31 depending therefrom are patentable over Iizuka. Claim 99 recites similar limitations to claim 1, including, *inter alia*, "an annealed dielectric layer . . . that has been annealed with a first oxidizing gas anneal process; and an upper electrode . . . which is an oxidized gas annealed layer formed over said annealed dielectric layer that has been annealed with a second oxidizing gas anneal process." For at least the same reasons as discussed with respect to claim 1, claim 99 is patentable over Iizuka. Accordingly, Applicants respectfully request that the 35 U.S.C. § 102(e) rejection of claims 1-3, 7-16, 18-25, 29-31 and 99 be withdrawn.

Claims 4, 5 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka in view of U.S. Patent No. 5,452,178 ("Emesh"). Applicants

resepectfully traverse this rejection.

Claims 4, 5 and 17 depend from claim 1 and should be similarly allowable with claim 1 for at least the reasons provided above with regard to claim 1, and on their own merits. As discussed above, Iizuka does not teach or suggest a capacitor comprising, *inter alia,* "a bottom conducting layer . . . an *annealed dielectric layer,* wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process,*" as recited in claim 1 (emphasis added).

Emesh does not supplement the inadequacy of Iizuka in this respect. The Office Action asserts that "it would have been obvious to one of ordinary skill in the art . . . to modify the bottom electrode of Iizuka with the metal alloy or conductive metal oxide material, as taught by Emesh, so as to provide an alternative material to make the bottom electrode." However, Iizuka *teaches away* from this combination. Iizuka discloses a "semiconductor device having a capacitor formed by a high dielectric insulation film and a *noble metal* upper electrode which are successively layered on a *noble metal* lower electrode." Col. 2, lines 28-31; Col. 2, lines 38-40. (Emphasis added). Iizuka specifically discloses that "[t]he lower electrode 28 *and* the upper electrode 28 are formed by a *noble metal film* such as Ru, Ir, and Pt." Col. 3, lines 38-40. (Emphasis added).

Since Iizuka teaches that *both* electrodes in the capacitor should consist of a *noble metal,* Iizuka teaches away from Emesh's metal alloy or conducting metal oxide for either the upper or lower electrodes in Iizuka and there is no motivation to combine the teachings of Iizuka and Emesh.

Since the cited references do not teach or suggest all the limitations of claim 1, claims 4, 5 and 17 depending therefrom are patentable over the reference. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 4, 5 and 17 be withdrawn.

Claims 6 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka in view of U.S. Patent No. 6,303,426 ("Alers"). Applicants respectfully traverse this rejection.

Claims 6 and 14 depend from claim 1 and should be similarly allowable with claim 1 for at least the reasons provided above with regard to claim 1, and on their own merits. As discussed above, Iizuka does not teach or suggest a capacitor comprising, *inter alia,* "a bottom conducting layer . . . an *annealed dielectric layer,* wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process,*" as recited in claim 1 (emphasis added).

Alers does not supplement the inadequacy of Iizuka in this respect. The Office Action asserts that "it would have been obvious to one of ordinary skill in the art . . . to modify the invention of Iizuka with the bottom electrode made of metal nitride, as taught by Alers, so as to provide an alternative material for the bottom electrode." However, as discussed above, Iizuka *teaches away* from this combination. As such, Alers cannot be combined with Iizuka since Iizuka teaches away from any material other than noble metals for a bottom electrode. Accordingly, the references do not teach or suggest all the limitations of claim 1 and claims 6 and 14 depending therefrom, and Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 6 and 14 be withdrawn.

Claims 26 and 27 stand rejected under 35 U.S.C. § 102(e) as anticipated by, or in the alternative, under 35 U.S.C. § 103(a) as obvious over Iizuka, in view of U.S. Patent No. 6,475,854 ("Narwankar"). Applicants respectfully traverse this rejection.

Claims 26 and 27 depend from claim 1 and should be similarly allowable with claim 1 for at least the reasons provided above with regard to claim 1, and on their own merits. As discussed above, Iizuka does not teach or suggest a capacitor comprising, *inter alia*, "a bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," as recited in claim 1 (emphasis added).

Narwankar does not supplement the inadequacy of Iizuka. Narwankar discloses a plasma enhanced annealed layer, but does not disclose "an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," as recited in claim 1. Since Iizuka and Narwankar do not teach or suggest all the limitations of claim 1, claims 26 and 27 depending therefrom are patentable over the reference. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 26 and 27 be withdrawn.

Claim 28 stands rejected under 35 U.S.C. § 102(e) as anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as obvious over Iizuka, in view of U.S. Patent No. 6,387,802 ("Marsh"). Applicants respectfully traverse this rejection.

At the outset, Marsh has a filing date of June 15, 2000, which is *after* the filing date of the present application. Thus, the subject matter of Marsh does not qualify as prior art.

Claim 28 depends from claim 1 and should be similarly allowable with claim 1 for at least the reasons provided above with regard to claim 1, and on their own merits. As discussed above, Iizuka does not teach or suggest a capacitor comprising, *inter alia,* "a bottom conducting layer . . . an *annealed dielectric layer,* wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process,*" as recited in claim 1 (emphasis added). Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claim 28 be withdrawn.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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